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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/904,750	07/13/2001	Christopher W. Jones	0325.00485	3331

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EXAMINER	
HUYNH, KIM T	

ART UNIT	PAPER NUMBER
2189	2

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/904,750	Applicant(s) JONES ET AL.	
	Examiner Kim T. Huynh	Art Unit 2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

The term "an assembly apparatus" in claim 1 is a relative term which renders the claim indefinite. The term "an assembly apparatus" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1- 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsunami et al. (Pub. No US20030191910)

As per claim 1(as best understood), Matsunami discloses a device comprising:

- A programmable logic device mounted to said assembly apparatus and comprising (i) a plurality of logic block clusters[0069] and (ii) a plurality of

routing channels configured to interconnect said logic block clusters; and [0008-0009], [0043-0045],

- A die mounted to said assembly apparatus and comprising a first communication channel (i) configured to convert between a first serial data signal and a first parallel data signal and (ii) coupled to a first of said routing channels to exchange said first parallel data signal with at least one of said logic block clusters. [0086-0090], (fig.18, wherein logic connection configuration, setup execution 5002, and fig.17, wherein FPC200233 receives command and convert into a frame configuration, exchange ID, Sequence ID, source ID and destination ID, such as 1st signal routes to channel 1, 2nd signal routes to channel 2, etc. and FPC200233 converts protocols of serial and parallel)

As per claim 2, Matsunami discloses wherein (i) said die further comprises a second communication channel configured to convert between a second serial data signal and a second parallel data signal and (ii) coupled to a second of said routing channels to exchange said second parallel data signal with at least one of said logic block clusters. [0086-0090], (fig.18, wherein logic connection configuration, setup execution 5002, and fig.17, wherein FPC200233 receives command and convert into a frame configuration, exchange ID, Sequence ID, source ID and destination ID, such as 1st signal routes to channel 1, 2nd signal routes to channel 2, etc. FPC200233 converts protocols of serial and parallel)

As per claim 3, Matsunami discloses wherein (i) said die further comprises a third communication channel configured to convert between a third serial data signal and a third parallel data signal and (ii) coupled to a third of said routing channels to exchange said third parallel data signal with at least one of said logic block clusters. [0086-0090] (fig.18, wherein logic connection configuration, setup execution 5002, and fig.17, wherein FPC200233 receives command and convert into a frame configuration, exchange ID, Sequence ID, source ID and destination ID, such as 1st signal routes to channel 1, 2nd signal routes to channel 2, etc. FPC200233 converts protocols of serial and parallel)

As per claim 4, Matsunami discloses wherein (i) said die further comprises a fourth communication channel configured to convert between a fourth serial data signal and a fourth parallel data signal and (ii) coupled to a fourth of said routing channels to exchange said fourth parallel data signal with at least one of said logic block clusters. [0086-0090] (fig.18, wherein logic connection configuration, setup execution 5002, and fig.17, wherein FPC200233 receives command and convert into a frame configuration, exchange ID, Sequence ID, source ID and destination ID, such as 1st signal routes to channel 1, 2nd signal routes to channel 2, etc. FPC200233 converts protocols of serial and parallel)

As per claim 5, Matsunami discloses wherein said die further comprises a second communication channel (i) configured to convert between a second serial data signal and a second parallel data signal and (ii) coupled to said first routing

channel to exchange said second parallel data signal with at least one of said logic block clusters. [0086-0090]

As per claim 6, Matsunami discloses wherein said first communication channel is further coupled to said first routing channel to receive a control signal from one of said logic block clusters.[0080], [0087-0088]

As per claim 7, Matsunami discloses wherein said control signal is configured as one of (i) a portion of said first parallel signal and (ii) an encoding selection signal. [0080],[0087-0088], wherein frame header implies portion of signal & frame configuration implies encoding signal)

As per claim 8, Matsunami discloses wherein said first communication channel is further coupled to said first routing channel to present a status signal to at least one of said logic block clusters. [0086-0087]

As per claim 9, Matsunami discloses wherein said status signal is configured as one of (i) a portion of said first parallel signal and (ii) a special character indicator. [0080], [0087-0088],

As per claim 10, Matsunami discloses wherein said die further comprises a second communication channel (i) configured to convert between a second serial data signal and a second parallel data signal and (ii) coupled to said first routing channel to receive said second parallel data signal and a control signal from one of said logic block clusters.

As per claim 11, Matsunami discloses a method of fabricating a device comprising the steps of:

(A) mounting a programmable logic device to an assembly apparatus, wherein said programmable logic device comprises (i) a plurality of logic block clusters and (ii) a plurality of routing channels configured to interconnect said logic block clusters; [0008-0009], [0043-0045]

(B) mounting a die to said assembly apparatus, wherein said die comprises a first communication channel configured to convert between a first serial data signal and a first parallel data signal; and [0086-0090]

© coupling said first communication channel to said first routing channel to exchange said first parallel data signal between at least one of said logic block clusters and said first communication channel. [0086-0090]

As per claim 12, Matsunami discloses the method further comprising the step of coupling a second communication channel of said die to a second of said routing channels to exchange a second parallel data signal between at least one of said logic block clusters and said second communication channel. [0086-0090]

As per claim 13, Matsunami discloses the method further comprising the step of coupling a third communication channel of said die to a third of said routing channels to exchange a third parallel data signal between at least one of said logic block clusters and said third communication channel. [0086-0090]

As per claim 14, Matsunami discloses the method further comprising the step of coupling a fourth communication channel of said die to a fourth of said routing channels to exchange a fourth parallel data signal between at least one of said logic block clusters and said fourth communication channel. [0086-0090]

As per claim 15, Matsunami discloses the method further comprising the step of coupling a second communication channel of said die to said first routing channel to exchange a second parallel data signal between at least one of said logic block clusters and said second communication channel. [0086-0090]

As per claim 16, Matsunami discloses the method further comprising the step of coupling said first receive channel to said first routing channel to receive a control signal from one of said logic block clusters. [0080], [0087-0088]

As per claim 17, Matsunami discloses the method further comprising the step of coupling said first receive channel to said first routing channel to present a status signal to at least one of said logic block clusters. [0080], [0087-0088]

As per claim 18, Matsunami discloses the method further comprising the step of coupling a second receive channel of said die to said first routing channel to receive a control signal from one of said logic block clusters. [0080], [0087-0089]

As per claim 19, Matsunami discloses a circuit comprising:

- Means for mounting a first programmable die and a second die; [0008-0009], wherein connecting implies mounting)
- Means for routing signals among a plurality of logic block clusters in said first programmable die; [0008-0009], [0043-0045]
- Means for converting between a first parallel data signal and a first serial data signal in said second die; and [0008-0009], [0043-0045]

- Means for coupling said means for converting to said means for routing to exchange said first parallel data signal between said means for converting and at least one of said logic block clusters. [0086-0090]

Conclusion

4.. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 8:30AM- 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815 or via e-mail addressed to [mark.rinehart@uspto.gov]. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9306 for regular communications and After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.

Kim Huynh

Nov. 29, 2003

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
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